Ryerson Polytechnic University
Department of Electrical and Computer Engineering
ELE538 – Microprocessor Systems

Final Examination a **December 16, 1998**

Name:________________________ **Student ID:** ____________ **Section:**______

Time: 3 hours Examiner: A.Lee

Closed-book except for 68HC11 Technical Data
Answer all questions on this paper
Use the same symbolic name for any internal registers as presented in the Data book.
Assume that these symbolic names have been declared properly already

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1. (**6 marks**)Consider the following pseudo-code and assembler code fragments. The left column contains assembler that may match one of the pseudo-code fragments in the right column. Each pseudo-code segment in the right column has an identifying letter; write that letter into the box of the assembler code that it corresponds to.

[ ]

```
foo: .ds 1
bar: .ds 10
 ldaa foo
 cmpa bar+2
 bhi L1
 inc foo
 bra done
L1: dec foo
done:
```

[ ]

```
foo: .ds 1
bar: .ds 10
 ldaa foo
 cmpa bar+4
 bls L1
 inc foo
 bra done
L1: dec foo
done:
```

[ ]

```
foo: .ds 1
bar: .ds 10
 ldaa foo
 cmpa bar+2
 bls  L1
 inc foo
 bra done
L1: dec foo
done:
```

A

```
unsigned char foo, bar[10];
if (foo > bar[2])
    foo++;
else
    foo--;
```

B

```
signed char foo, bar[10];
if (foo > bar[2])
    foo++;
else
    foo--;
```

C

```
unsigned char foo, bar[10];
if (foo <= bar[2])
    foo++;
else
    foo--;
```

```
foo: .ds 1
bar: .ds 10
      ldaa foo
L1:   cmpa bar+2
      bls done
      deca
      bra L1
done: staa foo
```

```
foo: .ds 1
bar: .ds 10
 ldaa foo
 cmpa bar+2
 bgt  L1
 dec foo
 bra done
L1: inc foo
done:
```

```
foo: .ds 1
bar: .ds 10
    ldaa foo
    cmpa bar+5
    bhs L1
    inc foo
    inc foo
L1: dec foo
done: ...
```

D

```
unsigned char foo;
unsigned char bar[10]

while(foo > bar[2])
  foo--;
```

E

```
unsigned char foo;
unsigned int bar[5];
if (foo > bar[2]>>8)
   foo++;
else
   foo--;
```

F

```
unsigned char foo;
unsinged int bar[5];

if (bar[2]&0xff > foo)
  foo++;
else
  foo--;
```

2. (**8 marks**)Consider Figure 1 shown below. The devices connected to the microprocessor bus include 8K ROM, 4K RAM and two devices: A and B. The table below summarizes the behavior of the internal locations (registers) of the two devices.

Device A, Internal locations 0 and 1	Readable and Writable
Device A, Internal locations 2	Read-only
Device A, Internal locations 3	Write-only
Device B, Internal locations 0–7	Readable and Writable
Device B, Internal locations 8,9,A, B	Read-only
Device B, Internal locations C, D, E. F	Write-only

For each of the instructions below, check the boxes ("Read", "Write", "Legal", "Illegal") that apply and fill in the "Internal location" and "Device" boxes.

For example, if the instruction causes a "read" cycle, check the **Read** box; if the address maps to a location that is indeed readable, check **Legal**. If the address maps to ROM, write **ROM** in the box after the word "Device". Similarly, use the words **RAM**, **DevA**, or **DevB** if the address maps to the "RAM", "Device A" or "Device B". Write the internal address (in **hexadecimal**) of the device that is accessed in the space after the word "location".

If more than one device is selected, mark it as "Illegal" and place an "X" in the Device and Location boxes. If **no** device is selected, mark it as illegal and place "NONE" in the Device and Location boxes.

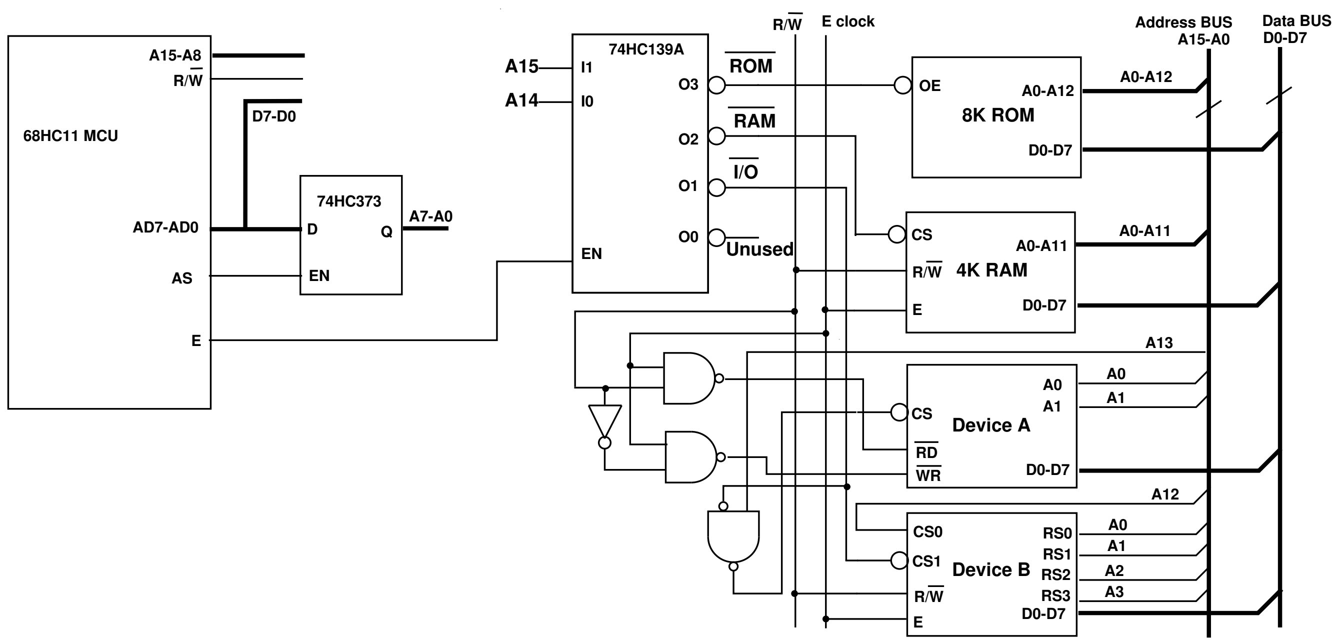

Figure 1: Memory-mapped devices (RAM, ROM, Device A, Device B)

`ldaa 0x6001`	Legal ☐	Illegal ☐	Read ☐	Write ☐	Device ☐	Internal location ☐
`staa 0x50A2`	Legal ☐	Illegal ☐	Read ☐	Write ☐	Device ☐	Internal location ☐
`ldab 0x8123`	Legal ☐	Illegal ☐	Read ☐	Write ☐	Device ☐	Internal location ☐
`ldaa 0xB123`	Legal ☐	Illegal ☐	Read ☐	Write ☐	Device ☐	Internal location ☐
`ldaa 0x7000`	Legal ☐	Illegal ☐	Read ☐	Write ☐	Device ☐	Internal location ☐
`staa 0xE000`	Legal ☐	Illegal ☐	Read ☐	Write ☐	Device ☐	Internal location ☐
`ldaa 0x4000`	Legal ☐	Illegal ☐	Read ☐	Write ☐	Device ☐	Internal location ☐
`ldaa 0x50BB`	Legal ☐	Illegal ☐	Read ☐	Write ☐	Device ☐	Internal location ☐

3. (**6 marks**)The waveform below in Figure 2 is viewed on a serial RS-232 link with the following parameters:

- Data speed: 1000 bps
- 7 data bits plus 1 Even parity bit
- 1 Stop bit

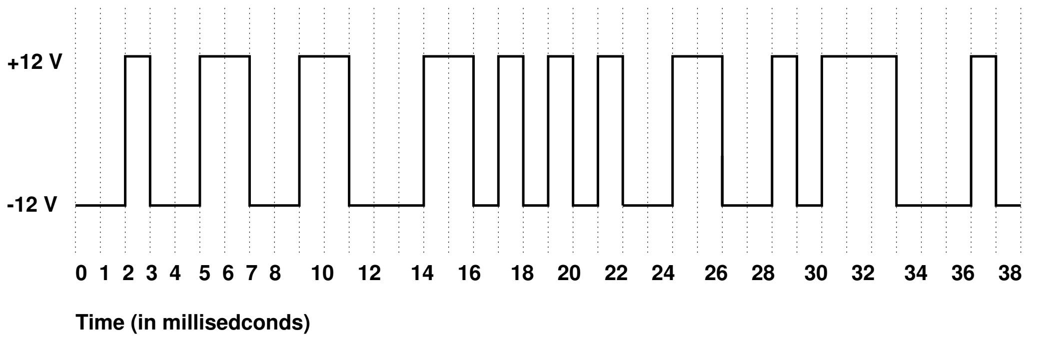

Figure 2: RS-232C Waveform

Assume that the 6811 SCI subsystem is reading this serial waveform (after conversion to TTL voltages). The 6811 software reads the "Serial Communications Data Register" at times 13 and 39 msec.

Check a box in each line indicating if the statement is true or false.

	True	False	
(a)	☐	☐	Character 1 is 0x33 (ignoring the parity bit)
(b)	☐	☐	Character 2 is 0x2A (ignoring the parity bit)
(c)	☐	☐	Character 1 has a parity error
(d)	☐	☐	Character 2 has a parity error
(e)	☐	☐	Character 3 has a parity error
(f)	☐	☐	A framing error is detected at a time between 8 and 14 msec.
(g)	☐	☐	A framing error is detected at a time between 22 and 28 msec.
(h)	☐	☐	A framing error is detected at a time between 35 and 40 msec.
(i)	☐	☐	An overrun error is detected at a time between 8 and 14 msec.
(j)	☐	☐	An overrun error is detected at a time between 22 and 28 msec.
(k)	☐	☐	An overrun error is detected at a time between 35 and 40 msec.

Which answers (if any) would change if the protocol required 2 stop bits? List the letter codes of the answers that would change (i.e. statements that were true before and would now be false or vice versa).

Would change: ☐

4. (**6 marks**)The following I/O subsystem (Figure 3) is used. Note that FF1 is negative-edge triggered, while FF2 is positive-edge triggered.

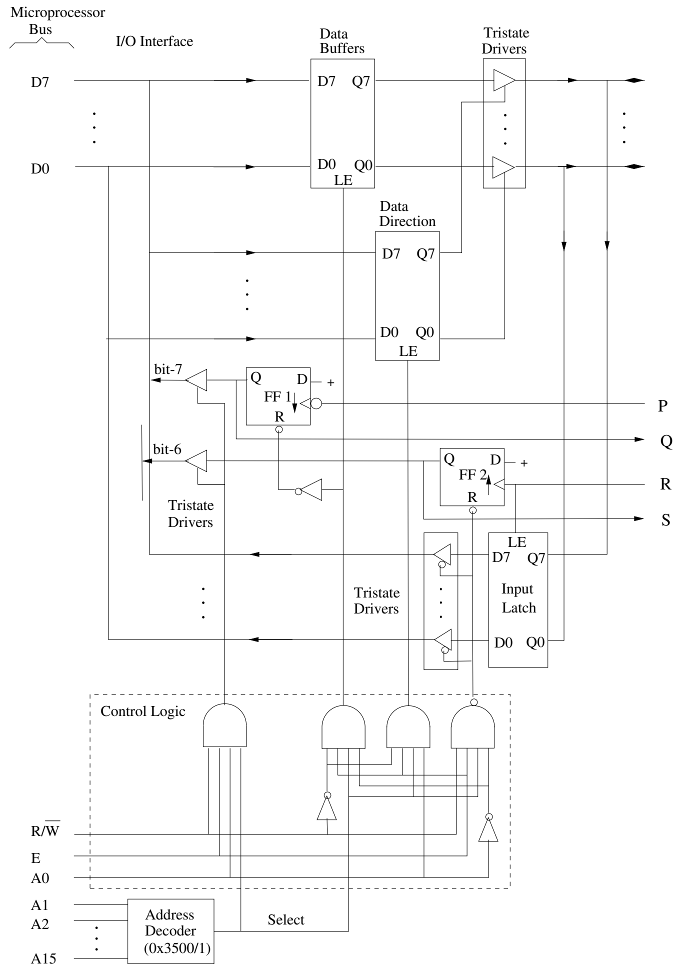

Figure 3: Peripheral hardware subsystem

(a) Indicate which signal corresponds to each of the following logical signals and whether the signal uses positive or negative logic.

i. DAV for data that is read from the port: ________ (Signal) _______ (Polarity)

ii. DAV for data that is written to the port: ________ (Signal) _______ (Polarity)

iii. DAC for data that is read from the port: ________ (Signal) _______ (Polarity)

iv. DAC for data that is written to the port: ________ (Signal) _______ (Polarity)

(b) What address must be read to determine the state of FF1 and FF2?

5. (**5 marks**)The A/D subsystem is to be set up for continuous scan mode of channel 1 only.

(a) Circle the statements that are true.

i. The sequence `tst 0x1030; bpl done` will jump to location done when a conversion has completed.

ii. The sequence `ldaa 0x1030; rola; bcs done` will jump to location "done" when a conversion has competed.

(b) Indicate which of the following registers should be initialized. You may assume that the initialization follows a Reset. If a register need not be initialized, draw a large "X" through it.

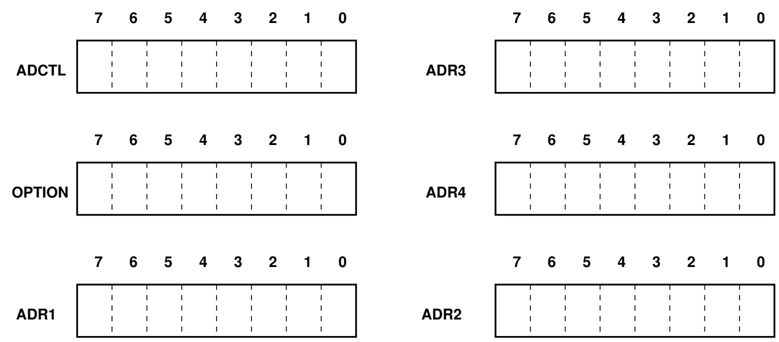

Figure 4: A/D registers

6. (**5 marks**)A delay can be implemented in software with the following C code:

```
void delay(void) {
     unsigned int i;
     for (i=0;i<N;i++);
     }
```

The output of the gcc6811 compiler indicated that the usage of *delay()* (where N is replaced by 100) is compiled into:

```
0010 BD 00 37       34     jsr _delay  ; CALL: R:*ZD0 = _delay (0 bytes) 6~
                    71 _delay:
                    73 ;;;  PROLOGUE for delay
0037 18 3C          75     pshy    ; Save stack frame                5~
0039 18 30          76     tsy ; Set current stack frame             4~
003B DE 00          77     ldx *ZD5                                  4~
003D 3C             78     pshx    ; pushed register *ZD5            4~
                    79 ;;;END PROLOGUE
003E CC 00 00       80     ldd #0                                    3~
0041 DD 00          81     std *ZD5    ; movhi: #0 -> *ZD5           4~
0043                82 L24:
0043 DE 00          83     ldx *ZD5                                  4~
0045 08             84     inx                                       3~
0046 DF 00          85     stx *ZD5    ; addhi3: *ZD5 by #1 -> *ZD5  4~
0048 DC 00          86     ldd *ZD5                                  4~
004A 1A 83 00 63    87     cpd #99 ; cmphi *ZD5 with #99             5~
004E 22 03          88     bhi .+5                                   3~
0050 7E 00 43       89     jmp L24 ; (bleu) long branch              3~
                    90 ;;;EPILOGUE
0053 38             91     pulx    ; Pulling register *ZD5           5~
0054 DF 00          92     stx *ZD5                                  4~
0056 18 38          93     puly    ; Restore stack frame             6~
0058 39             94     rts ; return from function                5~
                    96 ;;; END EPILOGUE for delay
```

A certain delay (in cycles) will be generated whenever *delay()* is called:

(a) Estimate this delay value. Ignore any overhead. (Show your calculation) **(2 marks)**

Estimate: | **cycles** |

(b) Calculate the exact total delay value by including all overhead. **(2 marks)**

Exact: | **cycles** |

(c) What is the new value of N that would yield a delay time closest to 10,000 cycles? **(1 mark)**

N:

7. (**4 marks**)A 68HC11 controller based system is required to communicate with another similar system using the on-board SCI facility. The required configuration are:

- full duplex serial communication
- 8N1 (i.e. 8-bit data, No parity, 1 stop bit) data format at 4800 baud, with system clock (E) running at 1 MHzK (i.e. the crystal frequency is 4 MHz).
- a single interrupt service routine to handle both transmit and receive operations (whenever one or both of TDRE and RDRF flags are set)

A programmer left some notes indicating what registers should be initialized what their values should be. Unfortunately, the programmer (who has since left the company) was working on several projects. Assume that the initialization is done following a Reset.

Circle all the initializations that apply to this problem and are correct. Mark an X though initializations that apply to the problem but are incorrect. Do not mark initializations that are unrelated to the problem.

(a) 0x102B should be 0b00110000
(b) 0x102D should be 0b00000000
(c) 0x102C should be 0b00000000
(d) 0x1030 should be 0b10010010
(e) 0x1022 should be 0b00101100

8. (**5 marks**)Two interrupt service routines are required. Routine A has a high priority and must always run to completion; routine B has a lower priority and should be interruptible by Routine A.

   For each of the following operations, indicate the order in which they should be done for both routines. If the operation is not applicable, mark an "X" in the corresponding box.

ISR-A Order	**ISR-B Order**	
		cli
		sei
		Handle request
		Acknowledge interrupt (i.e. clear the device flag)
		Verify source of interrupt

9. (**4 marks**)The timer sub-system of the 68hc11 is to be used to generate an interrupt every 10 ms on a system with a 1MHz clock. Assume that Output Compare register 2 is being used.

   Indicate which registers of the set CFORC, OC1M, OC1D, TCTL1, TCTL2, TMSK1, TFLG1, TMSK2 and TFLG2 have to be initialized and what values they should be initialized with. (Mark an X through registers that do not have to initialized for this application; you may assume that your initialization follows a Reset.

	7	6	5	4	3	2	1	0
OC1M								
TCTL2								
TCTL1								
TMSK1								
TFLG1								

	7	6	5	4	3	2	1	0
OC1D								
CFORC								
TMSK2								
TFLG2								