Ryerson Polytechnic University
Department of Electrical & Computer Engineering
ELE328 – Digital Systems

Test No. 1 **October 26, 1998**

Name: ______________________ **Section:** __________

Notes:

1. Time Limit: 1 hour and 50 minutes
2. Answer all questions in the space provided
3. Closed Book

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1. (a) Use a Karnaugh Map to find a minimum *sum of products* expression for the following logic function. **(3 marks)**

$$\mathbf{F(A,B,C,D) = \Sigma(0,3,9,13,14,15) + \Delta(10,11,12)}$$

(b) Implement this function using NAND gates and inverters only. **(3 marks)**

2. A synchronous circuit is to be designed using three (3) positive edge triggered D flip-flops. After an initial asynchronous active low $\overline{CLR}$, the circuit is to go through the following repetitive sequence.

Q_2	Q_1	Q_0
0	0	0
1	1	0
0	1	0
1	0	1
0	0	1
0	1	1
0	0	0

(a) Derive the logic equations for the three D inputs D_2 D_1 D_0. **(5 marks)**

(b) Draw the circuit using a minimum number of NAND gates and inverters, labelling all inputs and outputs. **(3 marks)**

(c) Draw the waveforms for the clock, $\overline{CLR}$ and outputs for the first 8 clock pulses following $\overline{CLR}$. **(3 marks)**

3. For the given input waveforms to the following latch, choose the correct output response.
(2 marks)

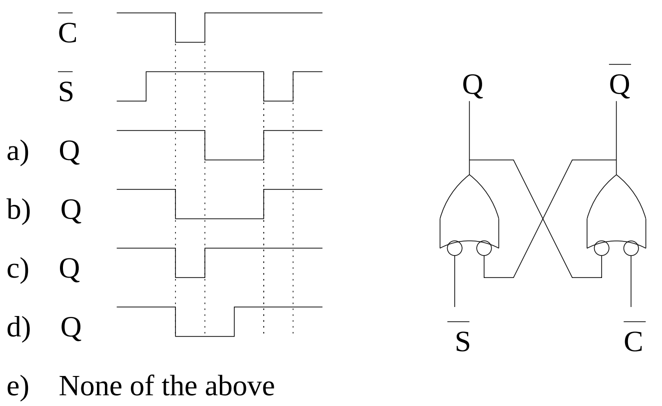

Figure 1:

4. Given the clock pulse signal and input waveform for the following circuit, select the correct output signal:
(2 marks)

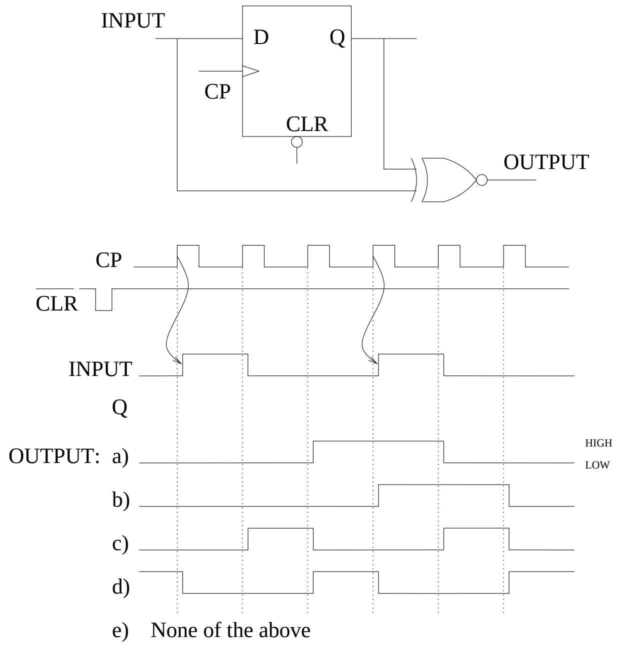

Figure 2:

5. Design a 1 out of 4 decoder that has an active low enable $\overline{En}$ and active low outputs, using NAND gates and inverters.

(1.5 marks)

6. Representing the above 1 out of 4 decoder as a single module, shown below, use the required number of modules and no additional gates to construct a 1 out of 16 decoder. Decode variables ABCD. Label **ALL** inputs and outputs. **(2.5 marks)**