Ryerson Polytechnic University
Department of Electrical & Computer Engineering
ELE328 – Digital Systems

Test No. 1 - Answers **October 22, 1997**

Name: _____ **Section:** _____

Notes:

1. Time Limit: 1 hour and 50 minutes
2. Answer all questions in the space provided
3. Closed Book

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1. A digital logic circuit inputs two 2-bit binary numbers $A = A_1\ A_0$ and $B = B_1\ B_0$ and produces the output $Z = Z_1\ Z_0$, where Z = A if A > B, Z = B if B > A and Z = 1 1 if A = B.

   (a) Construct a truth table for the system. **(1 mark)**

   (b) Draw the K-maps for both Z_1 and Z_0. **(2 marks)**

   (c) Derive the simplest Sum of Products expressions for Z_1 and Z_0. **(2 marks)**

A1	A0	B1	B0	Z1	Z0
0	0	0	0	1	1
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	1	1
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Table 1:

A1 A0 \ B1 B0	0 0	0 1	1 1	1 0
0 0	1	0	1	1
0 1	0	1	1	1
1 1	1	1	1	1
1 0	1	1	1	1

Z1 = B1 + A1 + A0B0 + /A0/B0

A1 A0 \ B1 B0	0 0	0 1	1 1	1 0
0 0	1	1	1	0
0 1	1	1	1	0
1 1	1	1	1	1
1 0	0	0	1	1

Z1 = /A1/B1 + A1B1 + A1A0 + B1B0

Z1 = /A1/B1 + A1B1 + /A1B0 + A0/B1

2. Given the following Register Circuit:

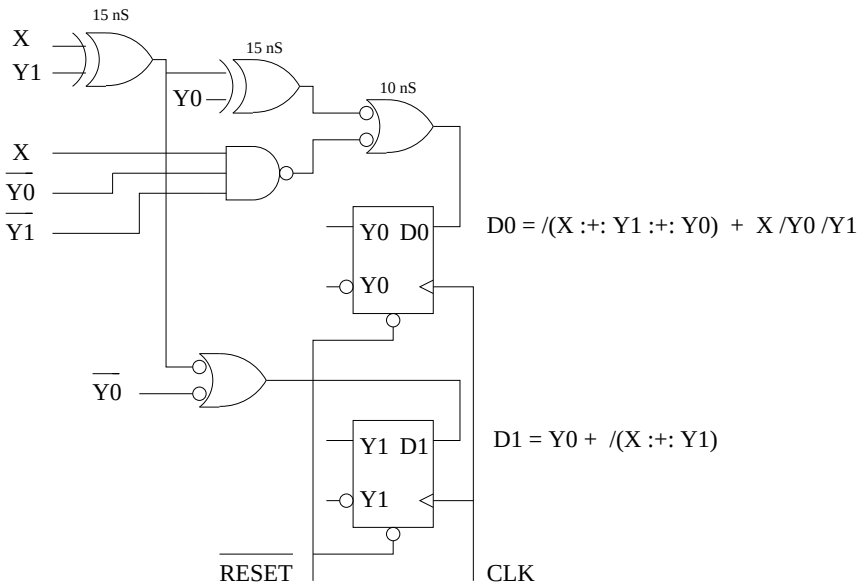


Figure 1: Synchronous Sequential Circuit

(a) Given the following timing parameters, calculate the maximum clock frequency. **(2 marks)**

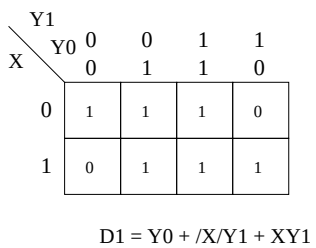
FF delay = 20 nS.
t_{setup} = 10 nS.
t_{hold} = 5 nS.
t_{NAND} = 10 nS.
t_{X-OR} = 15 nS.
t_w min = 30 nS.
Add 20% safety factor

$T_{min} = (20 + 15 + 15 + 10 + 10) \times 1.2nS.$

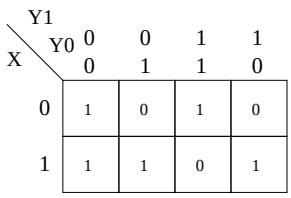
$f_{max} = 11.9MHz$

(b) For the above sequential synchronous circuit, derive the equations for D_0 and D_1 as functions of X, Y_0 and Y_1. Show answer on Figure 1. **(2 marks)**

(c) Place the functions for D_0 and D_1 on Karnaugh maps. **(2 marks)**



D1 = Y0 + /X/Y1 + XY1



D0 = /Y1/Y0 + /(X :+: Y1 :+: Y0)

Figure 2: Karnaugh Maps

(d) Construct a transition table for the above circuit. **(3 marks)**

PRESENT			NEXT	
X	Y1	Y0	D1	D0
0	0	0	1	1
0	0	1	1	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

Figure 3: Transition Table

(e) Derive the correct state diagram, assuming S0 = $\overline{Y_1}\,\overline{Y_0}$, S1 = $\overline{Y_1}\,Y_0$, S2 = $Y_1\,\overline{Y_0}$, S3 = $Y_1\,Y_0$. **(3 marks)**

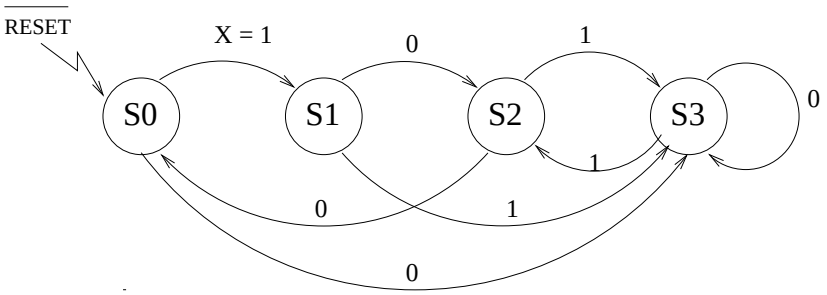
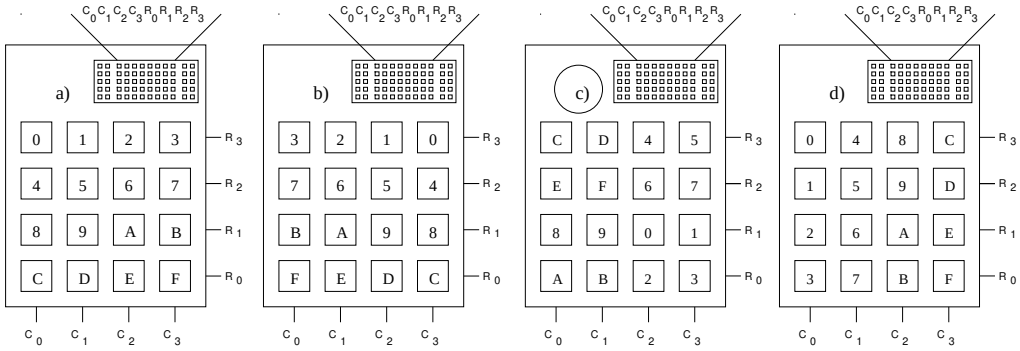


Figure 4: State Diagram

3. For the following hardware encoder circuit, the key arrangement must be:
(3 marks)



e) None of the above

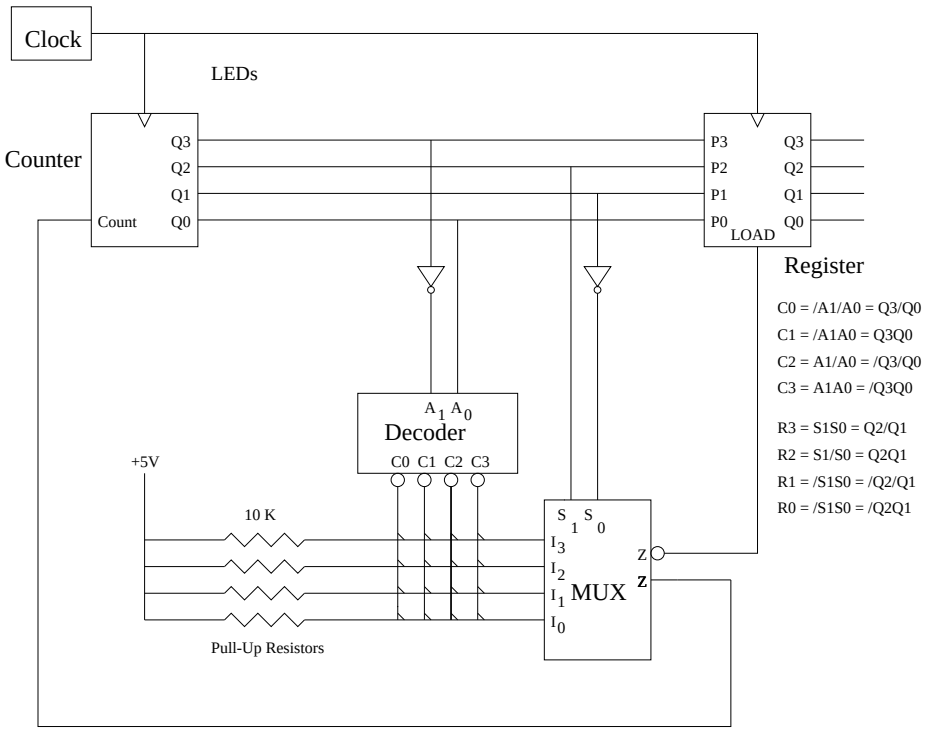


Figure 5:

4. Given the following Register Circuit:

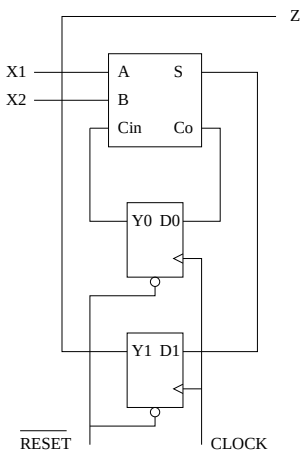


Figure 6: Synchronous Sequential Circuit

(a) Sketch the correct output waveforms at Cin, Co, S and Z in their proper time relationship to the following input waveforms. **(4 marks) Note:** Both flip-flops are initially set as indicated.

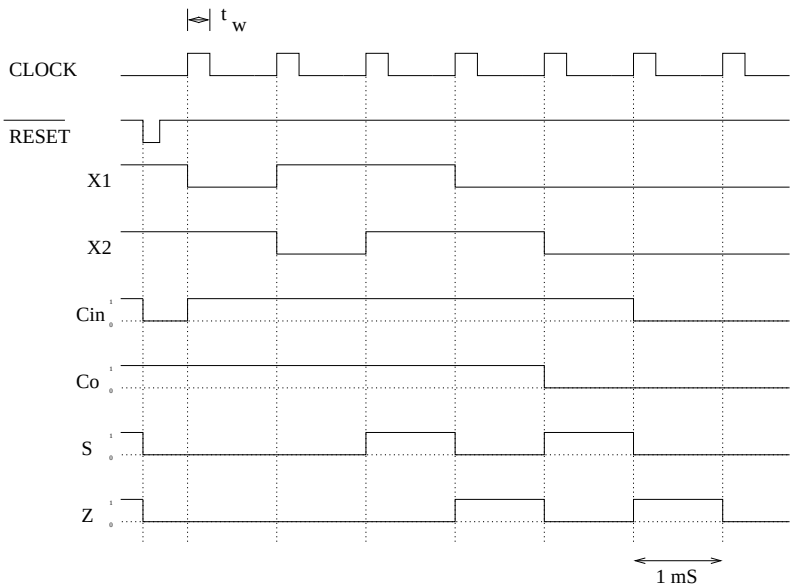


Figure 7: Waveforms

(b) What is the purpose of this circuit? **(1 mark)**
Serial addition of 2 binary numbers, LSB first.