Ryerson Polytechnic University
Department of Electrical & Computer Engineering
ELE328 – Digital Systems

Test No. 1 **October 24, 1996**

Name: ________________________ **Section:** __________

Notes:

1. Time Limit: 1 hour and 50 minutes
2. Answer all questions in the space provided
3. Closed Book

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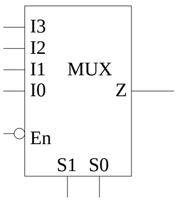
1. Design a digital logic circuit that compares 2-bit binary numbers $A = A_1\ A_0$ and $B = B_1\ B_0$ and produces the outputs $A = B$, $A > B$, $A < B$. Use the K-map to minimize each of the logic functions. Use NAND gates to implement the functions. **(5 marks)**

2. (a) Design a 4-to-1 multiplexer that has an active low enable $\overline{En}$ using NAND gates and inverters. **(2 marks)**

(b) Representing the above 4-to-1 multiplexer as a single module, shown below, use the required number of modules and no additional gates to construct a 16-to-1 multiplexer. Use select variables ABCD. Label **ALL** inputs. **(4 marks)**



3. Derive the correct logic expression for Z as realized by the following complementary switching circuit in Figure 1. **(2 marks)**

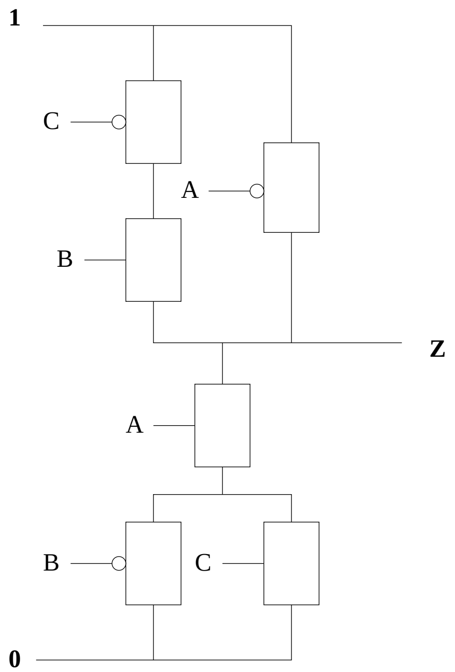
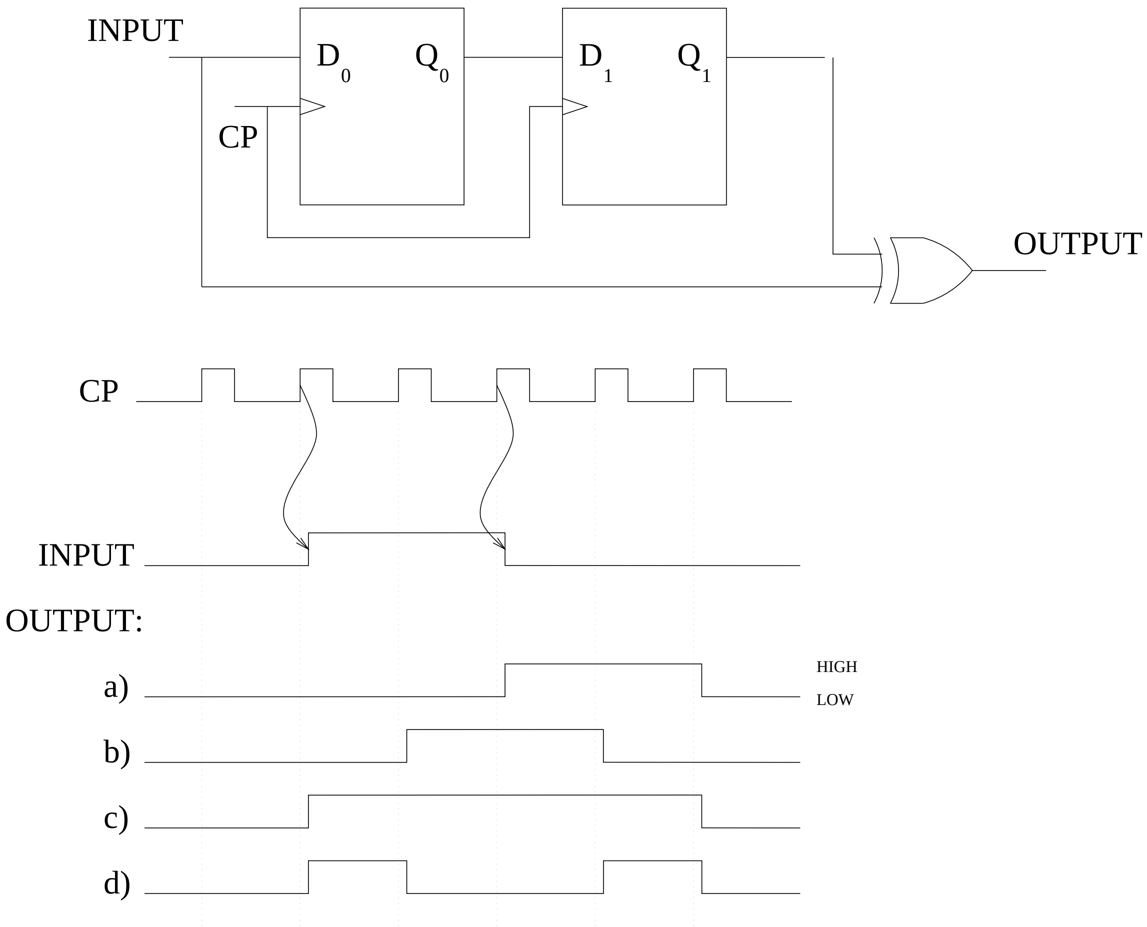


Figure 1:

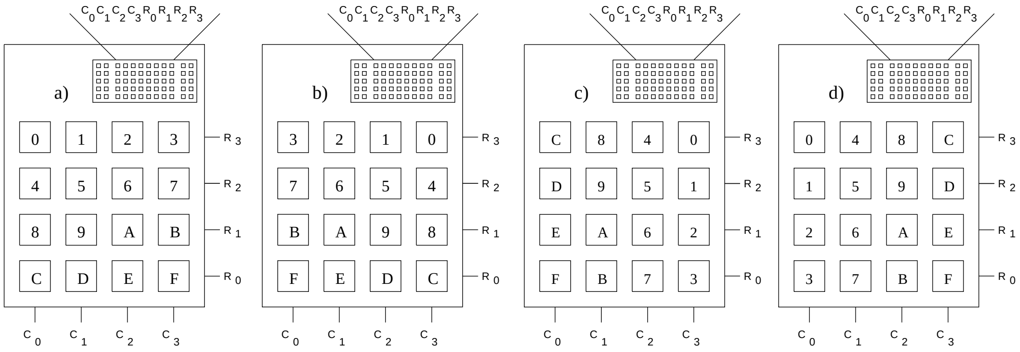
4. Given the following circuit, clock pulse signal and input waveform, circle the correct output signal:
Assume both flip-flops are initially reset. **(2 mark)**



e) None of the above

Figure 2:

5. For the following hardware encoder circuit, the key arrangement must be:
(1 mark)



e) None of the above

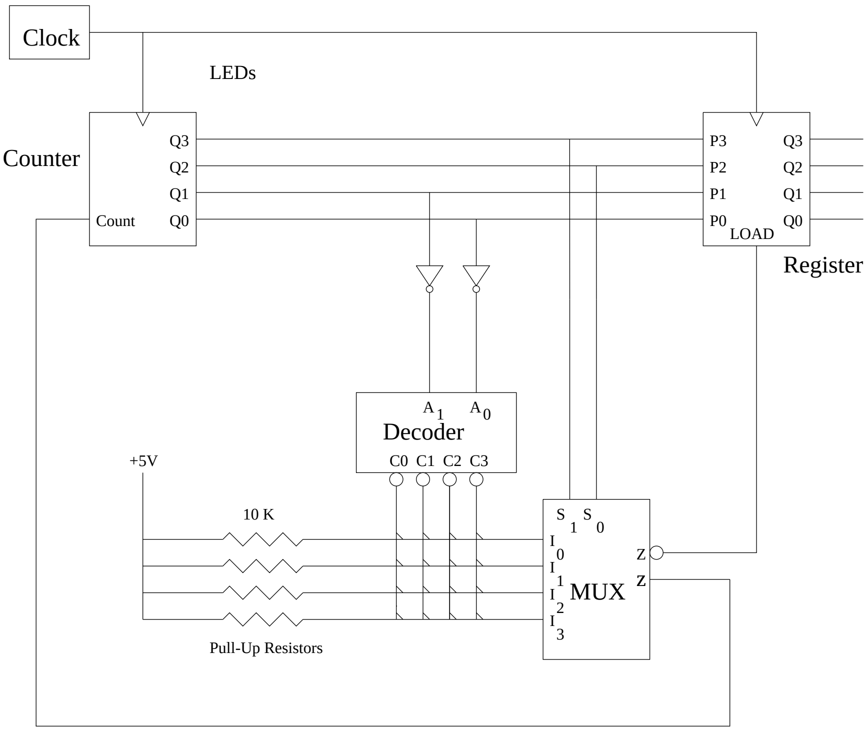


Figure 3:

6. Given the following Register Circuit:

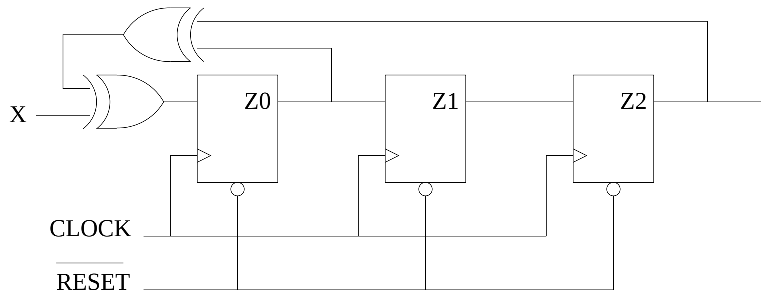


Figure 4: Synchronous Sequential Circuit

(a) Sketch the correct output waveforms at Z_0, Z_1 and Z_2 in their proper time relationship to the following input waveforms. **(3 marks)**

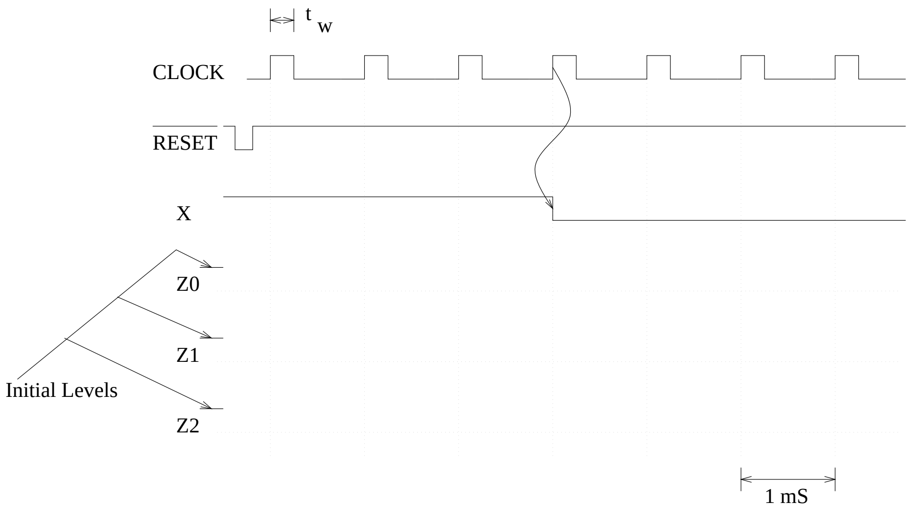


Figure 5: Waveforms

(b) Indicate whether the above circuit is a Moore or Mealy type. **(1 mark)**

(c) Given the following timing parameters, calculate the maximum clock frequency. **(2 marks)**

FF delay = 20 nS.
t_{setup} = 10 nS.
t_{gate} = 7 nS. f_{max} = ?
t_w min = 30 nS.
Add 25% safety factor

(d) Analyse the circuit, construct a transition table and derive the correct state diagram. **(3 marks)**

PRESENT				NEXT		
IN	Z0	Z1	Z2	Z0	Z1	Z2
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

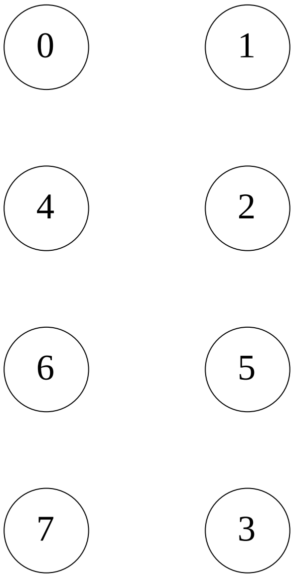


Figure 6: