Ryerson Polytechnic University
Department of Electrical & Computer Engineering
ELE328 – Digital Systems

Test No. 1 **October 30, 1995**

Name: ________________________ **Section:** __________

Notes:

1. Time Limit: 1 hour and 50 minutes
2. Answer all questions
3. Closed Book

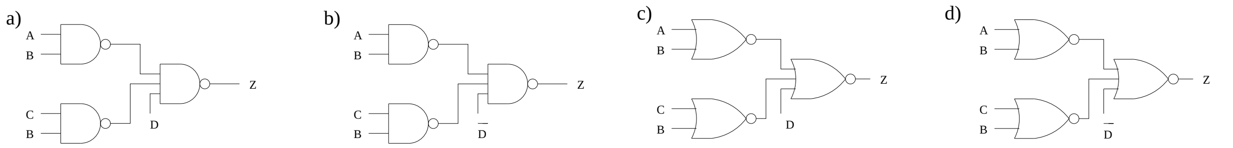
Part A: Multiple choice questions. Circle the correct answer

Problems 1 to 8:

1. Which of the following logic circuits represents the given logic equation?

$$Z = A \cdot B + C \cdot B + D$$

(1 mark)



e) None of the above

Figure 1:

2. Which of the following logic equations implements the given truth table?
(1 mark)

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

a) $Z = A + B + C$

b) $Z = \overline{A}\,\overline{B} + \overline{A}\,\overline{C} + \overline{B}\,\overline{C}$

c) $Z = \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\,\overline{C}$

d) $\overline{Z} = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}BC + A\overline{B}\,\overline{C}$

e) None of the above

Figure 2:

3. For the given input waveforms to the following latch, choose the correct output response. **(1 mark)**

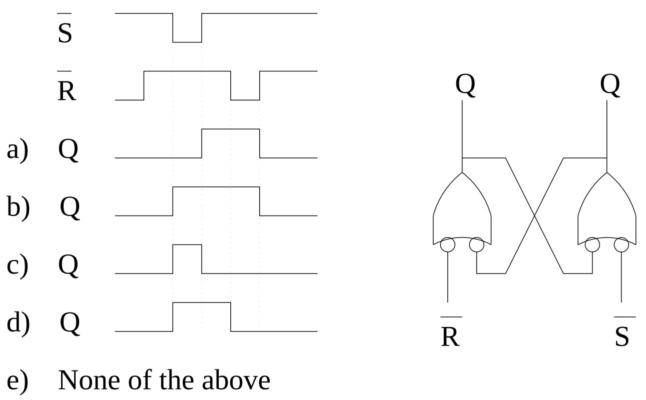


Figure 3:

4. Which of the following logic equations applies to the accompanying circuit? **(1 mark)**

a) $\overline{Z} = A\overline{B} + \overline{A}B$

b) $\overline{Z} = AB + \overline{A}\,\overline{B}$

c) $Z = A\overline{B} + \overline{A}B$

d) $Z = \overline{AB + \overline{A}\,\overline{B}}$

e) None of the above

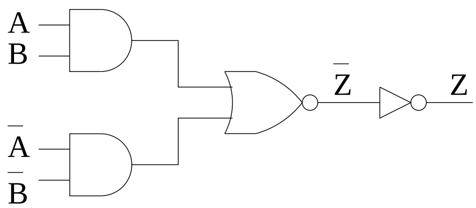


Figure 4:

5. **(1 mark)**

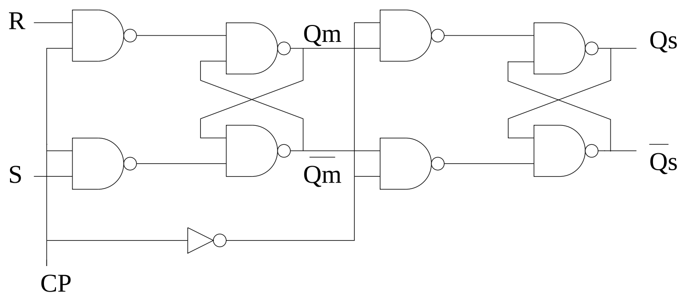


Figure 5:

Refering to the above circuit, which of the following statements is true?:

(a) A HIGH on CP disables master and slave

(b) A LOW on CP disables master and enables slave

(c) A HIGH on CP enables master and slave

(d) A LOW on CP enables master and slave

(e) None of the above

6. Given the following circuit, clock pulse signal and input waveform, select the correct output signal: **(1 mark)**

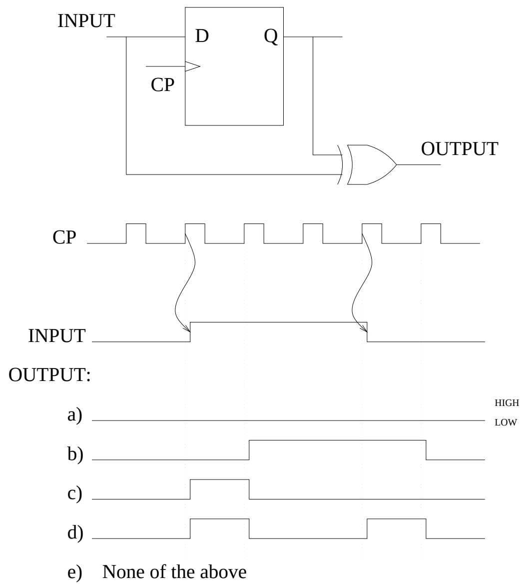
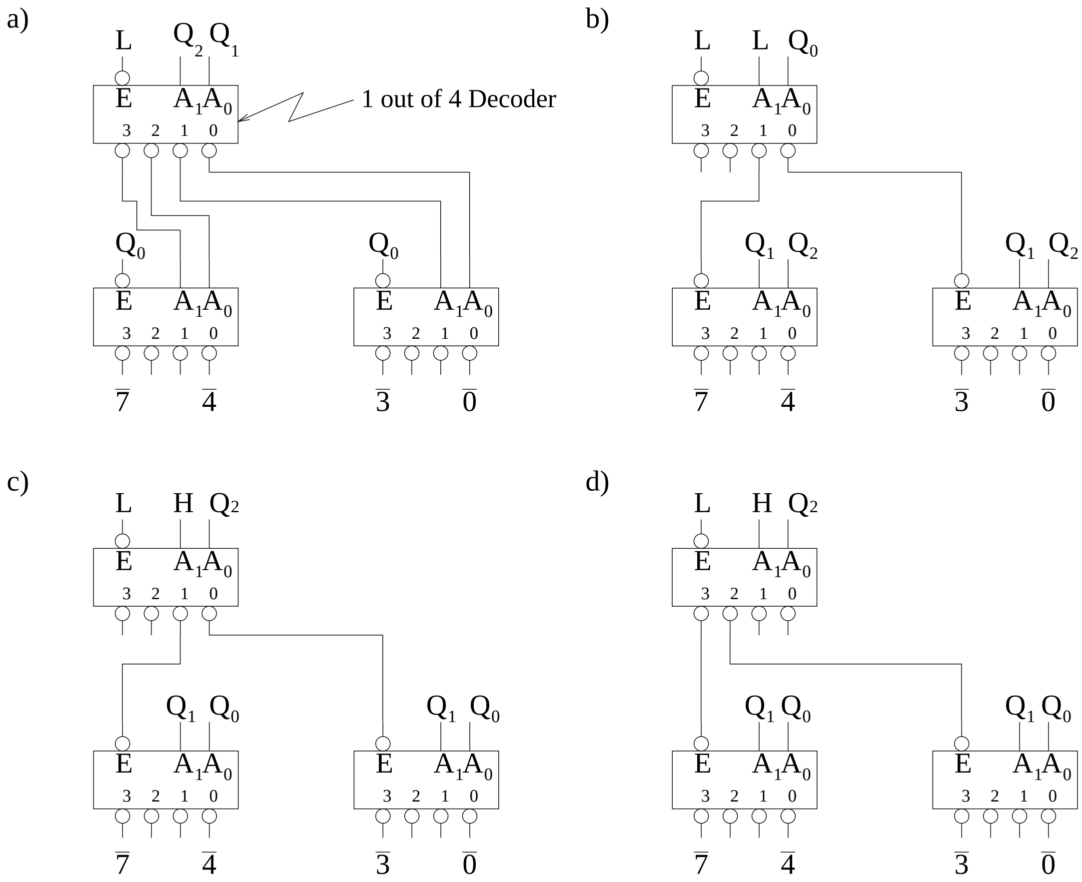


Figure 6:

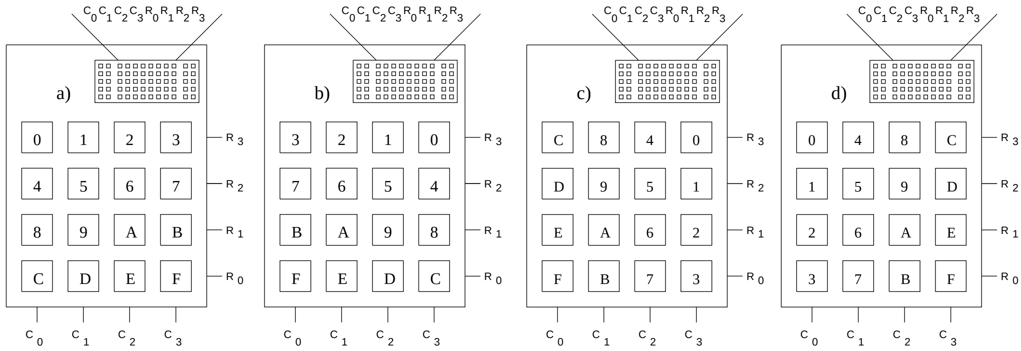
7. Which one of the following circuits will correctly decode the three bit binary signal, $Q_2Q_1Q_0$? **(1 mark)**



e) None of the above

Figure 7:

8. For the following hardware encoder circuit, the key arrangement must be:
(1 mark)



e) None of the above

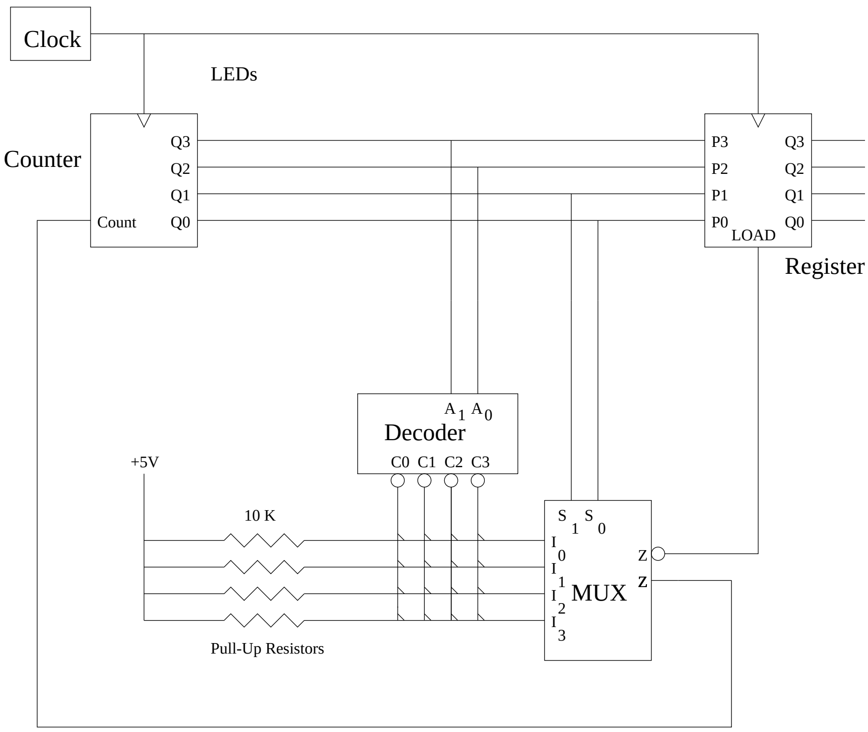


Figure 8:

Part B: Answer in the space provided

9. Convert the decimal number 43.75 into each of the following codes: **3 marks**

   (a) binary

   (b) hexadecimal

   (c) Binary Coded Decimal

10. Use a Karnaugh Map to find a <u>m</u>inimum *product of sums* expression for the following logic function.

$$\mathbf{F(A,\ B,\ C,\ D) = \prod(0,\ 1,\ 4,\ 9,\ 13,\ 14,\ 15) + \triangle(2,\ 5,\ 6,\ 11)}$$

Implement this function using NAND gates and inverters only. **4 marks**

11. Given the following synchronous sequential circuit:

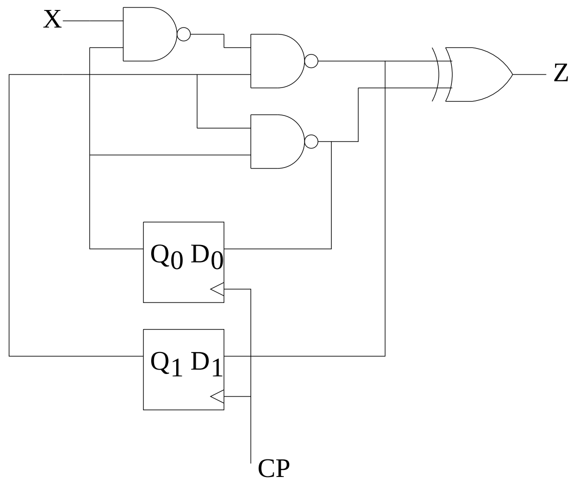


Figure 9: Synchronous Sequential Circuit

(a) Calculate the maximum frequency of operation assuming:
t_{w-min} = 20 nS (Min. CP width).
t_{ff-min} = 25 nS (Delay from D to Q or CP to Q).
t_{pd-min} = 10 nS (NAND Gate delay).
t_{pd-min} = 15 nS (Exclusive Or Gate delay).
t_{su-min} = 10 nS (FF setup time).
t_{h-min} = 5 nS (FF hold time).
Add 20 % to T_{min} as a safety factor. **(3 marks)**

(b) Complete the following Transition Table for the circuit in Fig. 9.

	Input	Present State		Next State		Output
State	X	Q_1	Q_0	Q_1^+	Q_0^+	Z
S0	0	0	0			
S1	0	0	1			
S2	0	1	0			
S3	0	1	1			
S0	1	0	0			
S1	1	0	1			
S2	1	1	0			
S3	1	1	1			

Figure 10: Transition Table

(4 marks)

(c) Complete the following State Diagram for the circuit in Fig. 9.

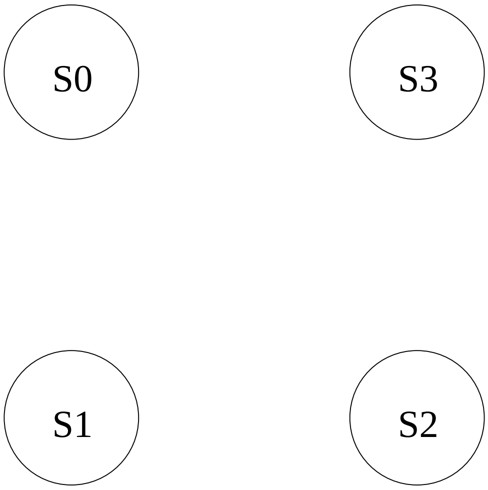


Figure 11: State Diagram

Make sure you indicate both the primary input and primary output, X/Z, for each of the transitions. **(3 marks)**