Ryerson Polytechnic University
Department of Electrical & Computer Engineering
ELE328 – Digital Systems

Test No. 1 **October 30, 1995**

Part A: Multiple choice questions.
1. b) 2. c) 3. d) 4. a) 5. b) 6. d) 7. d) 8. d)

Part B:

1. Convert the decimal number 43.75 into each of the following codes: **3 marks**

   (a) binary 101011.11

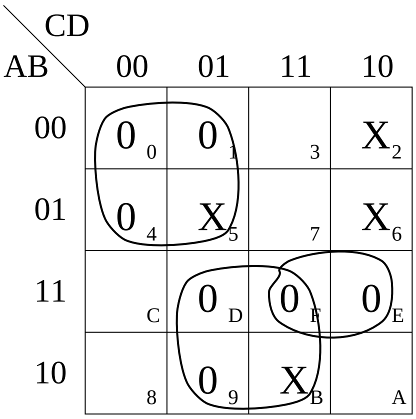
   (b) hexadecimal 2B.C

   (c) Binary Coded Decimal 0100 0011. 0111 0101

2. Use a Karnaugh Map to find a minimum *product of sums* expression for the following logic function.

$$\mathbf{F(A,\ B,\ C,\ D) = \prod(0,\ 1,\ 4,\ 9,\ 13,\ 14,\ 15) + \triangle(2,\ 5,\ 6,\ 11)}$$

   Implement this function using NAND gates and inverters only. **4 marks**



$$F = (A + C)(C + \overline{D})(\overline{A} + \overline{B} + \overline{C})$$

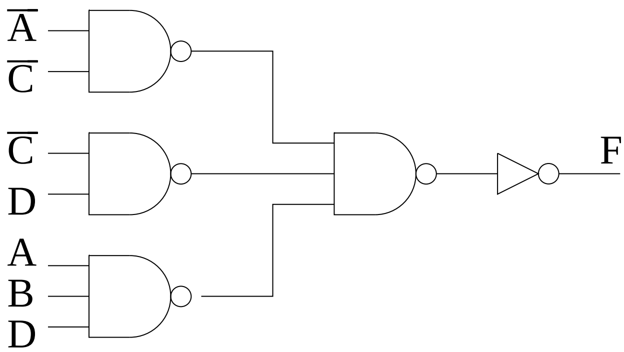
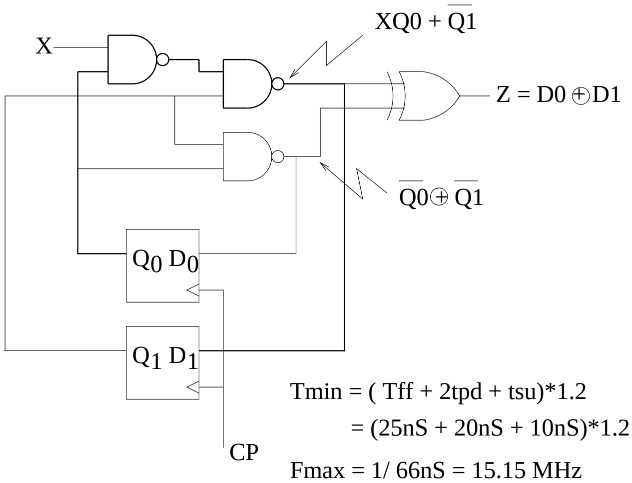


Figure 1: Question 10.

3. Given the following synchronous sequential circuit:



Tmin = (Tff + 2tpd + tsu)*1.2
= (25nS + 20nS + 10nS)*1.2 = 66nS

Fmax = 1/ 66nS = 15.15 MHz

Figure 2: Synchronous Sequential Circuit

(a) Calculate the maximum frequency of operation assuming:
t_{w-min} = 20 nS (Min. CP width).
t_{ff-min} = 25 nS (Delay from D to Q or CP to Q).
t_{pd-min} = 10 nS (NAND Gate delay).
t_{pd-min} = 15 nS (Exclusive Or Gate delay).
t_{su-min} = 10 nS (FF setup time).
t_{h-min} = 5 nS (FF hold time).
Add 20 % to T_{min} as a safety factor. **(3 marks)**

(b) Complete the following Transition Table for the circuit in Fig. 9.

	Input	Present State		Next State		Output
State	X	Q_1	Q_0	Q_1^+	Q_0^+	Z
S0	0	0	0	1	1	0
S1	0	0	1	1	1	0
S2	0	1	0	0	1	1
S3	0	1	1	0	0	0
S0	1	0	0	1	1	0
S1	1	0	1	1	1	0
S2	1	1	0	0	1	1
S3	1	1	1	1	0	1

Figure 3: Transition Table

(4 marks)

(c) Complete the following State Diagram for the circuit in Fig. 9.

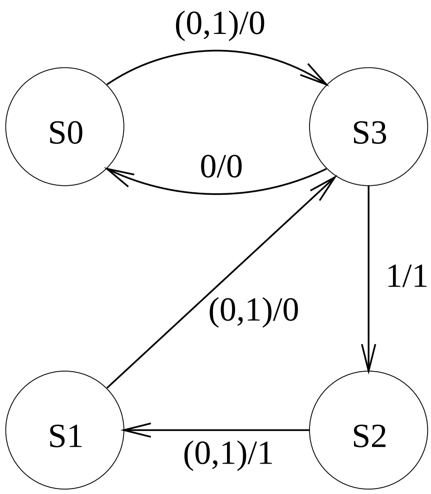


Figure 4: State Diagram

Make sure you indicate both the primary input and primary output, X/Z, for each of the transitions. **(3 marks)**