Ryerson Polytechnic University
Department of Electrical & Computer Engineering
ELE328 – Digital Systems

Final Examination **December 4, 1997**

Name:______________________________ **Section:**____________

Time: 2 1/2 hours
Examiners: D.Hawkes, P. Hiscocks
Answer all the following questions in the space provided.
Full marks 43.

1. Given the following circuit connection and level change at point A:

   Sketch the waveforms at A, B, C and OUT derived from the following circuit assuming the timing parameters as given. **(6 marks)**

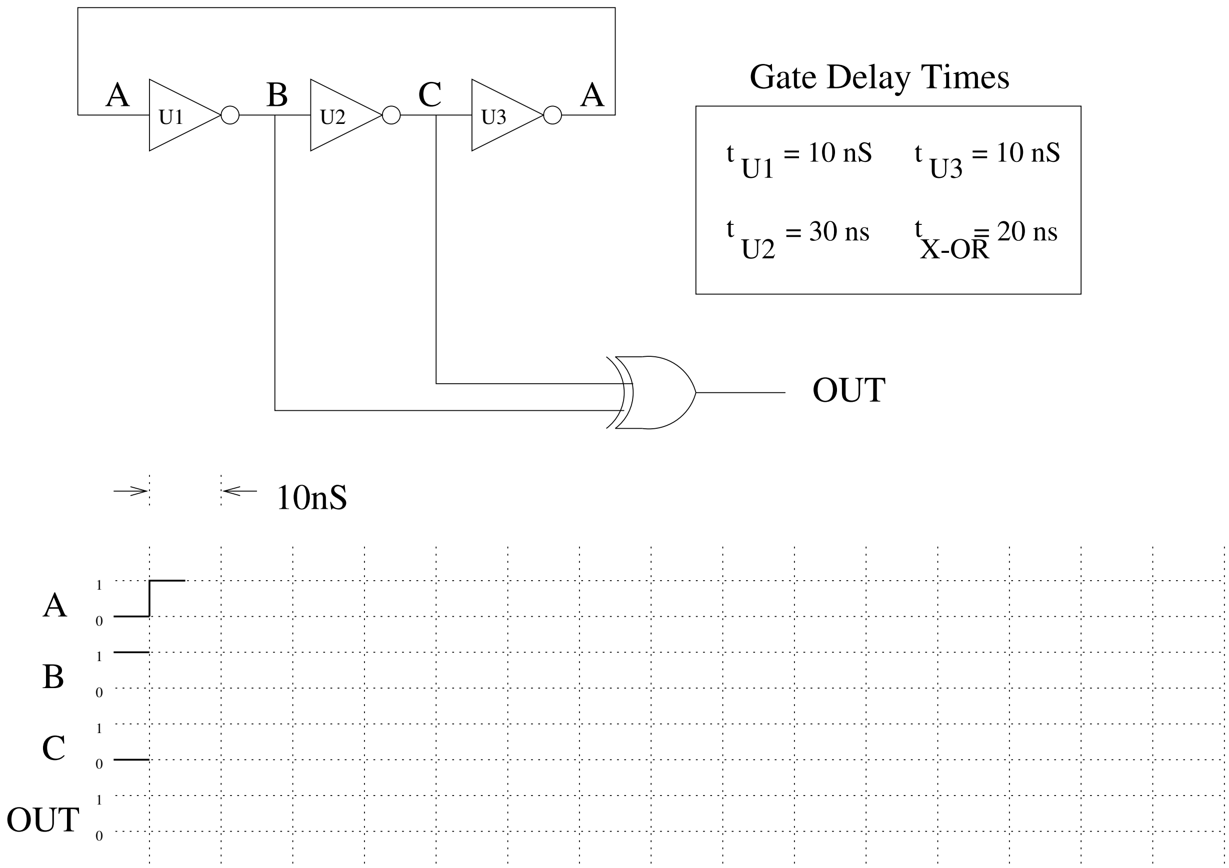

Figure 1: Synchronous Circuit

2. A priority encoder produces a binary output $Z = Z_1 Z_0$ representing the highest active input of the group I_3, I_2, I_1, and I_0. Eg. Z = 1 1 when $I_3 = 1$. As well, a FLAG output is 1 when any one of the inputs is active.

   (a) Determine the minimized logic functions for the outputs Z_1, Z_0 and FLAG. **(7 marks)**

   (b) Draw the encoder using a minimum number of NAND gates. **(3 marks)**

3. Design and draw the synchronous sequential circuit which will implement the following conditions:

   When control variable K = 0, outputs Q_2 Q_1 Q_0 are to sequence through the divide by 4 sequence 0 0 1, 0 1 1, 1 1 0, 1 0 1. When K = 1, outputs Q_2 Q_1 Q_0 are to sequence through the divide by 6 sequence 1 1 1, 1 1 0, 1 0 0, 0 0 0, 0 0 1, 0 1 1. For states common to the two sequences, a change in K should cause a smooth transition to the other sequence. For states unique to a sequence, a change in K should cause a transition to the beginning of the other sequence.

   (a) Draw a state diagram labelling all states and transitions. **(4 marks)**

   (b) Using the classical method, define your state variables and draw the transition and excitation tables using D f-f's with asynchronous clear. **(4 marks)**

(c) Show the required input equations and the final circuit using a minimum number of NAND gates and flip-flops. **(6 marks)**

(d) What happens next in your design if state 0 1 0 exists after power on? **(1 mark)**

4. Using the following memory module:

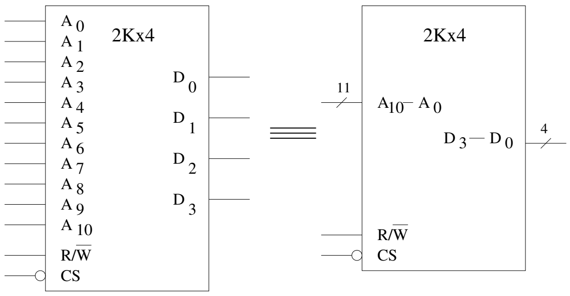

Figure 2: Memory module

(a) Design a memory circuit which will have 4 Kilo bytes of memory, (4K x 8). **(4 marks)**
Note: Standard TTL modules are available to be used in your design.

(b) Label the range of addresses for each module in the circuit using HEX values. **(2 marks)**

5. The diagram of a microcontrolled calculating machine is shown in the figure 3. Contents of the Read Only Memory are shown in figure 4.

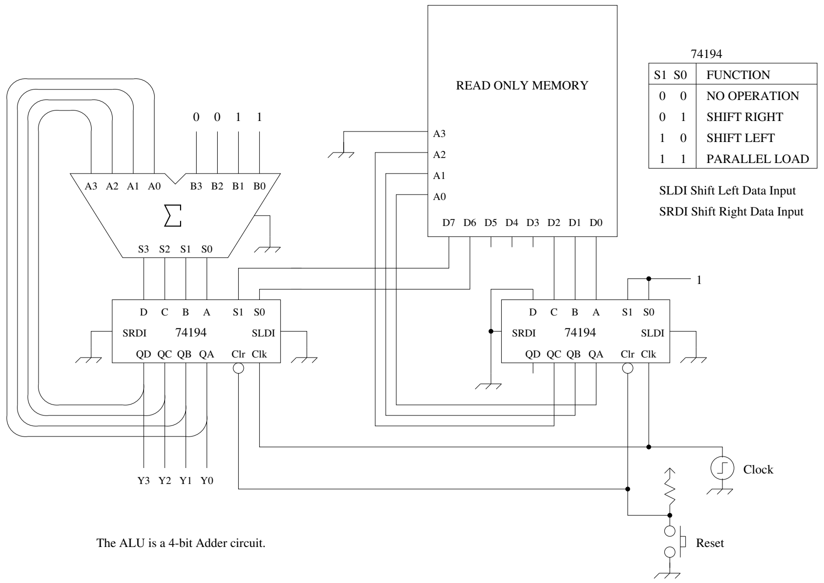

Figure 3: Calculating Machine

Read Only Memory Contents

Address	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	0	0	1
1	1	1	0	0	0	0	1	0
2	1	1	0	0	0	0	1	1
3	1	0	0	0	0	1	0	0
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0

Figure 4: Read Only Memory

The machine is reset with the pushbutton, at a time between two edges of the clock. Thereafter, the machine is allowed to run continuously.

(a) What is the value of Y after 15 clock cycles? **(4 marks)**

(b) Draw a state diagram for this machine. **(2 marks)**