Ryerson Polytechnic University
Department of Electrical & Computer Engineering
ELE328 – Digital Systems

Final Examination **December 8, 1995**

Name:______________________________ **Section:**____________

Time: 2 1/2 hours
Examiners: D.Hawkes, N.Mekhiel
Answer all the following questions in the space provided

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1. Given the following positive-edge triggered D-type flip-flop circuit connections and input waveform:

   (a) Sketch the waveforms for Q and Y in the space provided. **Note:** Your sketches must take into account the following timing parameters. **(8 marks)**

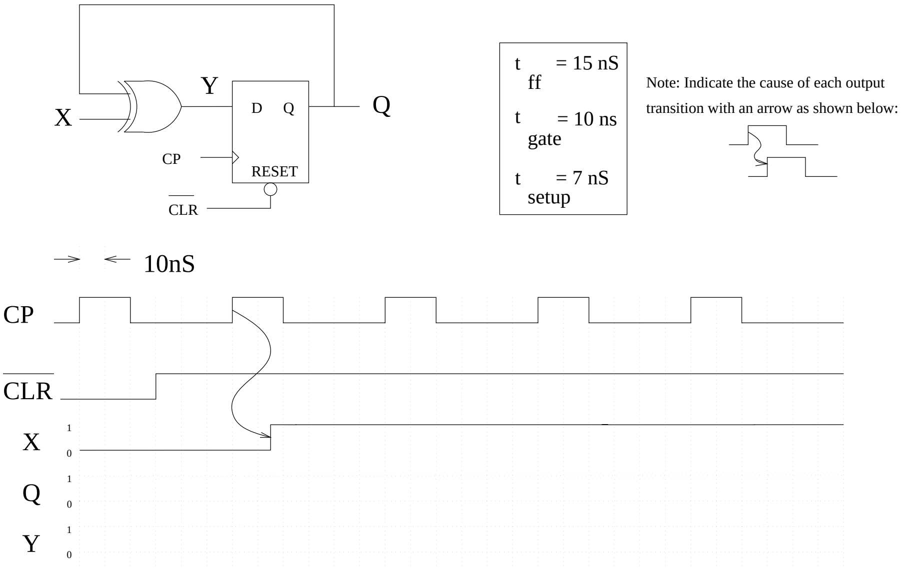
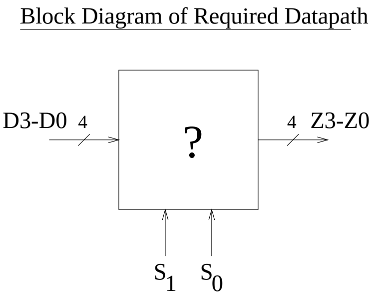


Figure 1: Synchronous Circuit

   (b) Estimate the maximum clock rate of this circuit assuming a 20% safety factor. **(2 marks)**

2. Using the block diagrams for any standard TTL modules (list of available devices given below), design the circuit to implement the datapath function as specified in figure 2. **(10 marks)**

   Available TTL modules: 4 to 1 MUXs, 1 of 4 decoders, 4-bit Universal registers, Full Adders, inverters, Nand gates.



Datapath Function Table

S_1	S_0	Z
0	0	0
0	1	D
1	0	/D
1	1	D plus 1

Figure 2: Datapath Design

3. Design a circuit that monitors a 2-bit number A_1A_0 and which actives an opening relay Z when the sequence 023 (00, 10, 11) is detected. The circuit will return to the initial state if either a wrong sequence is entered or upon completion of a correct sequence. The circuit should contain an asynchronous reset to the initial state. Your design should include a state table, state diagram, excitation table and final circuit which uses a **minimum** number of gates. **(10 marks)**

   Note: You may continue your work on the following blank page.

Question 3 Cont'd

4. The processor in figure 4 is the one used in project 9. It uses an ALU whose functions are listed in figure 5. **(5 marks)**

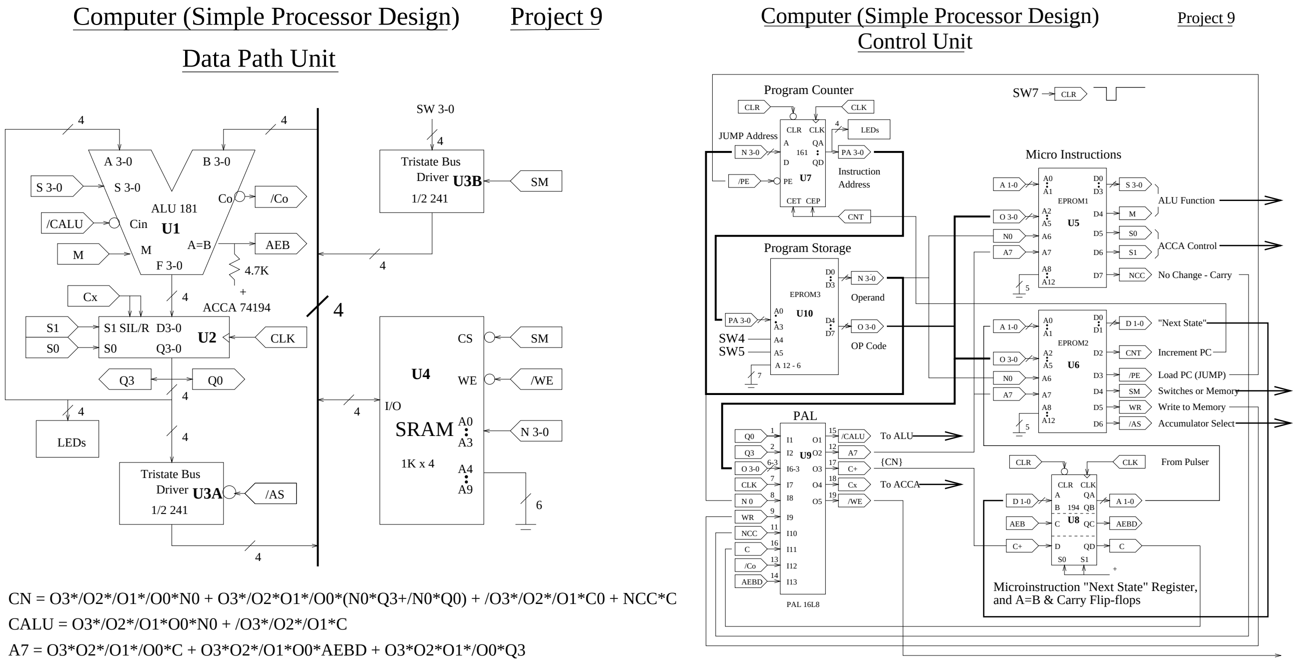
   (a) Determine the contents of the Program Counter PC, Accumulator ACCA, and the carry bit C, after the execution of each of the following instructions, given initial conditions for EACH of the instructions as follows:

Before each of the following instructions, the initial conditions are:

Sw = 1011 C = 1 PC = 0010 ACCA 0110 M(2) = 1010

	PC	ACCA	C
(i) INPA			
(ii) RORA			
(iii) JCS 1011			
(iv) SETA			
(v) ADDA 2			

Figure 3:



CN = O3*/O2*/O1*/O0*N0 + O3*/O2*O1*/O0*(N0*Q3+/N0*Q0) + /O3*/O2*/O1*C0 + NCC*C

CALU = O3*/O2*/O1*O0*N0 + /O3*/O2*/O1*C

A7 = O3*O2*/O1*/O0*C + O3*O2*/O1*O0*AEBD + O3*O2*O1*/O0*Q3

Figure 4: Processor

Arithmetic and logic functions performed by the 74181 ALU

				M = 1	M = 0 Arithmetic operations	
S_3	S_2	S_1	S_0	Logic functions	/Cn = 1 (no carry)	/Cn = 0 (with carry)
0	0	0	0	F = /A	F = A	F = A plus 1
0	0	0	1	F = /(A + B)	F = A + B	F = (A + B) plus 1
0	0	1	0	F = /A*B	F = A + /B	F = (A + /B) plus 1
0	0	1	1	F = 0	F = minus 1 (2's comp)	F = 0
0	1	0	0	F = /(A*B)	F = A plus A*/B	F = A plus A*/B plus 1
0	1	0	1	F = /B	F = (A + B) plus A*/B	F = (A +B) plus A*/B plus 1
0	1	1	0	F = A XOR B	F = A minus B minus 1	F = A minus B
0	1	1	1	F = A*/B	F = A * /B minus 1	F = A * /B
1	0	0	0	F = /A + B	F = A plus A*B	F = A plus A*B plus 1
1	0	0	1	F = /(A XOR B)	F = A plus B	F = A plus B plus 1
1	0	1	0	F = B	F = (A + /B) plus A*B	F = (A+/B) plus A*B plus 1
1	0	1	1	F = A*B	F = A*B minus 1	F = A*B
1	1	0	0	F = 1	F = A plus A	F = A plus A plus 1
1	1	0	1	F = A + /B	F = (A + B) plus A	F = (A + B) plus A plus 1
1	1	1	0	F = A + B	F = (A + /B) plus A	F = (A + /B) plus A plus 1
1	1	1	1	F = A	F = A minus 1	F = A

Figure 5: ALU Function Table

(b) Write a program to input 2 4-bit numbers from the switches and store the sum in address 2 and the difference in address 3. The program is to start at location 0000_{16} and return there to repeat the process. Fill in the following table with both source code and object code (HEX) together with instruction addresses (HEX). See available instruction set on the next page. **(5 marks)**

ADDRESS HEX	Object Code HEX	Source Code
0000		

Figure 6: RECS Program

Processor Instruction Set

- **0 0 0 0** $N_3N_2N_1N_0$, ADDA N : ACCA := ACCA + (N) + C.
- **0 0 0 1** $N_3N_2N_1N_0$, SUBA N : ACCA := ACCA - (N) - /C. Note: /C = Borrow Bit
- **0 0 1 0 X X X X**, INPA : load accumulator with input data from the switches, ACCA := (Sw)
- **0 0 1 1** $N_3N_2N_1N_0$, LDAA N : load accumulator with the contents of memory location N.
- **0 1 0 0** $N_3N_2N_1N_0$, STAA N : store ACCA into memory location N.
- **0 1 0 1** $N_3N_2N_1N_0$, JMP N : jump to program address N.
- **0 1 1 0** $N_3N_2N_1N_0$, ANDA N : AND the contents of N with ACCA and store in ACCA.
- **0 1 1 1** $N_3N_2N_1N_0$, ORA N : OR the contents of N with ACCA and store in ACCA.
- **1 0 0 0 X X X 0**, CLC : clear carry bit (C = 0).
- **1 0 0 0 X X X 1**, SEC : set carry bit (C = 1).
- **1 0 0 1 X X X 0**, DECA : decrement ACCA.
- **1 0 0 1 X X X 1**, INCA : increment ACCA.
- **1 0 1 0 X X X 0**, RORA : rotate ACCA right (Q_3 := C and C := Q_0). (Note: In your circuit Q_3 is on the left whereas in the 74194 specs, Q_3 is considered to be the rightmost bit).

- **1 0 1 0 X X X 1**, ROLA : rotate ACCA left (Q_0 := C and C := Q_3).
- **1 0 1 1 X X X X**, NOP : No operation or user defined instruction.
- **1 1 0 0** $N_3N_2N_1N_0$, JCS N : jump to program address N if carry set.
- **1 1 0 1** $N_3N_2N_1N_0$, JEQ N: jump to program address N if A = B.
  Note: ALU must be in subtract mode and CALU clear (borrow = 1) to make F = 1111 (AEB HIGH) when A = B. For these instructions, A = ACCA and B = switches (input).
- **1 1 1 0** $N_3N_2N_1N_0$, JMI N : jump to program address N if ACCA -ve (Q_3 = 1).
- **1 1 1 1 X X X 0**, CLRA : ACCA := 0000.
- **1 1 1 1 X X X 1**, SETA : ACCA := 1111.

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Final Examination **December 10, 1996**

Name:____________________________ **Section:**___________

Time: 2 1/2 hours
Examiners: D.Hawkes, P. Hiscocks
Answer all the following questions in the space provided.
Full marks 40, (45 marks available; 5 mark bonus possible).

1. Given the following positive-edge triggered D-type flip-flop circuit connection and input waveform:

   Sketch the output waveforms derived from the following circuit assuming the timing parameters as given. **(10 marks)**

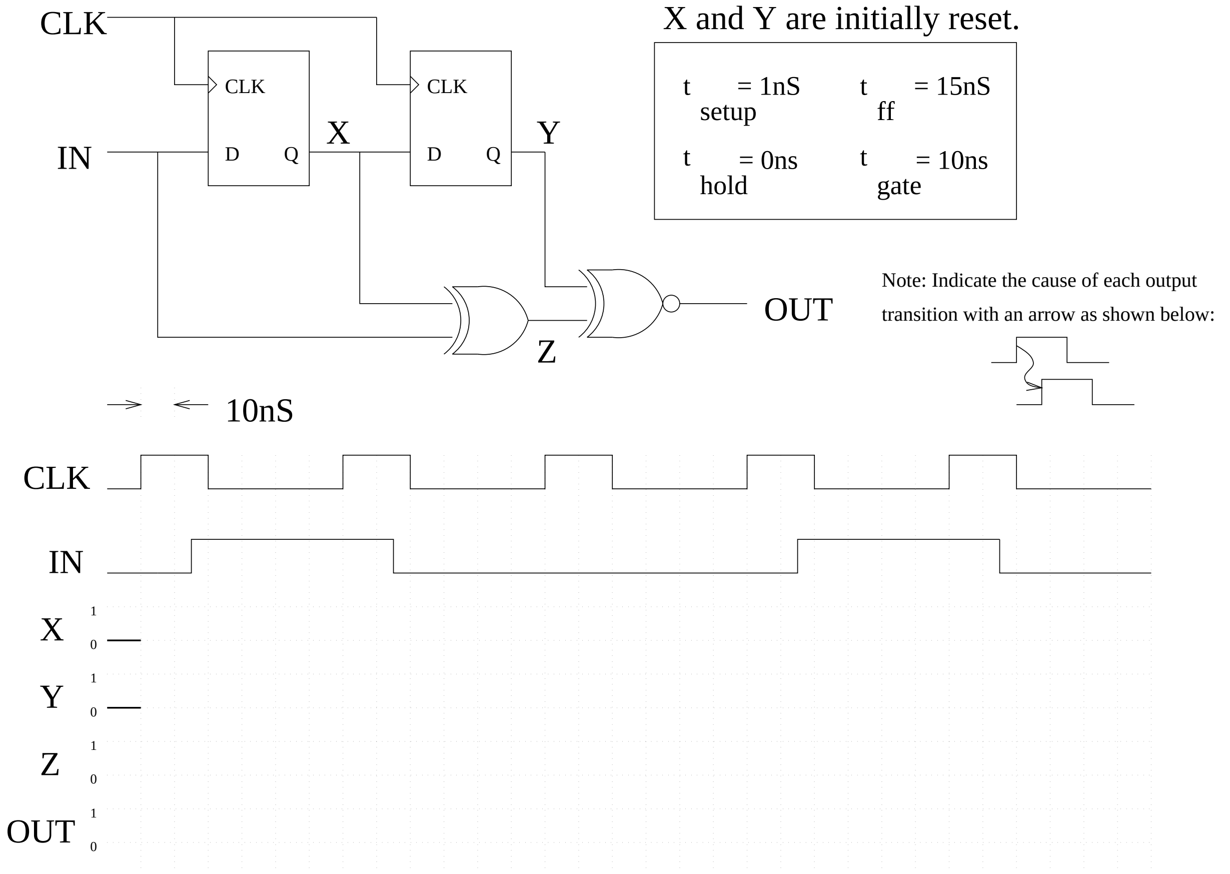
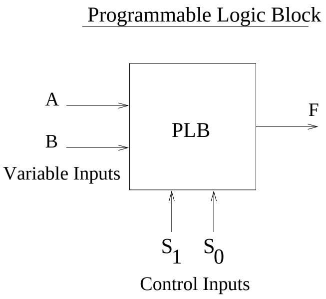


Figure 1: Synchronous Circuit

2. A programmable logic block (PLB) is to be designed with FOUR different selectable functions:


Programmable Logic Block

Function Table

S_1	S_0	F
0	0	0
0	1	$A \cdot B$
1	0	1
1	1	$A + B$

Figure 2: PLB Design

(a) Determine the minimized logic function for F. **(5 marks)**

(b) Draw the logic function using a minimum number of NAND gates. **(5 marks)**

3. Design and draw the synchronous sequential circuit which will implement the following conditions:

   Relay Z_0 is to be activated when input variables X_1 and X_0 sequence through the combinations, 10, 11 and 01 after a reset condition. If the sequence is broken, the circuit should return to its reset state, otherwise the circuit must be reset manually to return to its initial state.

   (a) Draw a state diagram labelling all states, transitions and outputs. **(4 marks)**

   (b) Using the classical method, (min. state variables), define your state variables and draw the transition and excitation tables. You may may use either D f-f's or JK f-f's with asynchronous clear and preset. **(4 marks)**

   (c) Show the required input equations and the final circuit. **(3 marks)**

   Note: You may continue your work on the following blank page.

Question 3 Cont'd

4. The processor in figure 4 is the one used in project 9. It uses an ALU whose functions are listed in figure 5 and the instruction set given on the page following. **(5 marks)**

   Determine the contents of the Program Counter PC, Accumulator ACCA, and the carry bit C, after the execution of each of the following instructions, given initial conditions for EACH of the instructions as follows:

Each of the following instructions has initial conditions as given:

Sw = 1011 C = 0 PC = 0010 ACCA 0110 M(2) = 1010

	PC	ACCA	C
(i) ADDA S			

Sw = 1100 C = 1 PC = 1100 ACCA 0101 M(2) = 0101

	PC	ACCA	C
(ii) RORLA			

Sw = 0110 C = 1 PC = 1010 ACCA 0110 M(2) = 1010

	PC	ACCA	C
(iii) JEQ 0011			

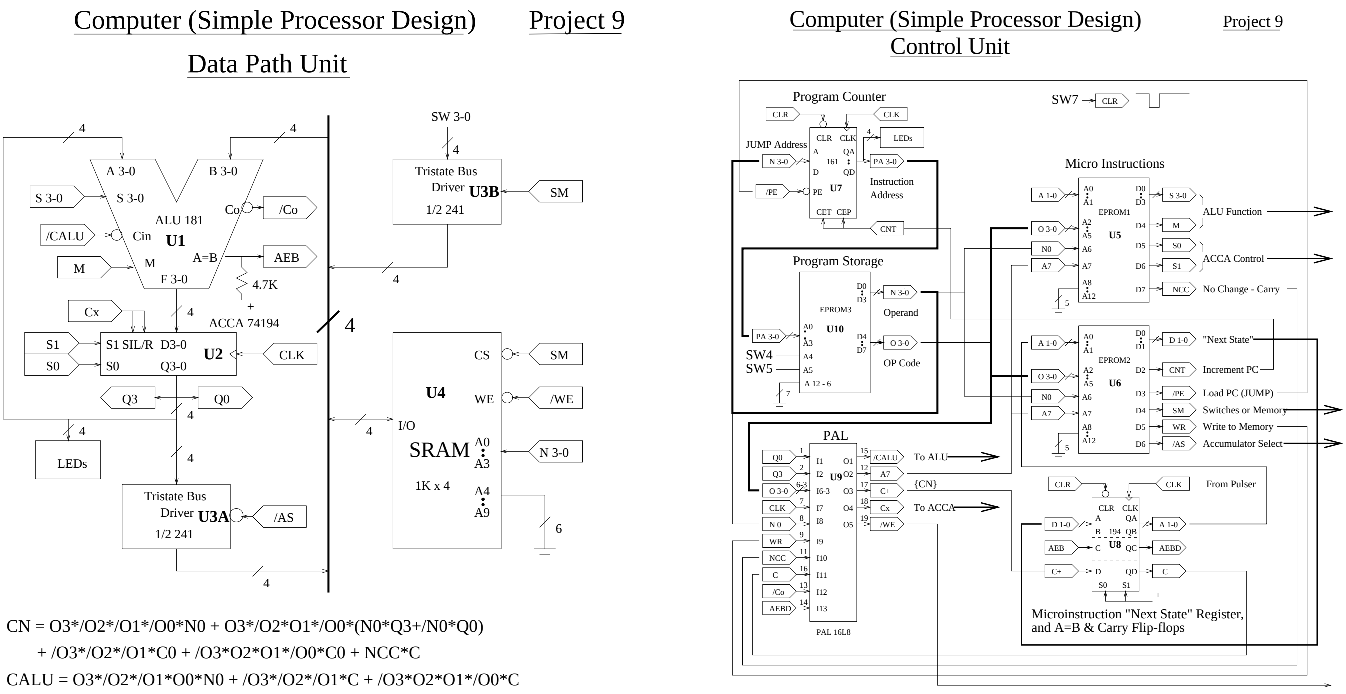
Sw = 1011 C = 1 PC = 0010 ACCA 0110 M(2) = 1010

	PC	ACCA	C
(iv) SETA			

Sw = 1000 C = 0 PC = 0010 ACCA 0110 M(2) = 0111

	PC	ACCA	C
(v) SUBA 2			

Figure 3:



CN = O3*/O2*/O1*/O0*N0 + O3*/O2*O1*/O0*(N0*Q3+/N0*Q0)
+ /O3*/O2*/O1*C0 + /O3*O2*O1*/O0*C0 + NCC*C

CALU = O3*/O2*/O1*O0*N0 + /O3*/O2*/O1*C + /O3*O2*O1*/O0*C

A7 = O3*O2*/O1*/O0*C + O3*O2*/O1*O0*AEBD + O3*O2*O1*/O0*Q3

Figure 4: Processor

Arithmetic and logic functions performed by the 74181 ALU

					M = 0 Arithmetic operations	
S_3	S_2	S_1	S_0	M = 1 Logic functions	/Cn = 1 (no carry)	/Cn = 0 (with carry)
0	0	0	0	F = /A	F = A	F = A plus 1
0	0	0	1	F = /(A + B)	F = A + B	F = (A + B) plus 1
0	0	1	0	F = /A*B	F = A + /B	F = (A + /B) plus 1
0	0	1	1	F = 0	F = minus 1 (2's comp)	F = 0
0	1	0	0	F = /(A*B)	F = A plus A*/B	F = A plus A*/B plus 1
0	1	0	1	F = /B	F = (A + B) plus A*/B	F = (A +B) plus A*/B plus 1
0	1	1	0	F = A XOR B	F = A minus B minus 1	F = A minus B
0	1	1	1	F = A*/B	F = A * /B minus 1	F = A * /B
1	0	0	0	F = /A + B	F = A plus A*B	F = A plus A*B plus 1
1	0	0	1	F = /(A XOR B)	F = A plus B	F = A plus B plus 1
1	0	1	0	F = B	F = (A + /B) plus A*B	F = (A+/B) plus A*B plus 1
1	0	1	1	F = A*B	F = A*B minus 1	F = A*B
1	1	0	0	F = 1	F = A plus A	F = A plus A plus 1
1	1	0	1	F = A + /B	F = (A + B) plus A	F = (A + B) plus A plus 1
1	1	1	0	F = A + B	F = (A + /B) plus A	F = (A + /B) plus A plus 1
1	1	1	1	F = A	F = A minus 1	F = A

Figure 5: ALU Function Table

Processor Instruction Set

- **0 0 0 0** $N_3N_2N_1N_0$, ADDA N : ACCA := ACCA + (N) + C.
- **0 0 0 1** $N_3N_2N_1N_0$, SUBA N : ACCA := ACCA - (N) - /C. **Note:** /C = Borrow Bit
- **0 0 1 0 X X X X**, INPA : load accumulator with input data from the switches, ACCA := Sw
- **0 0 1 1** $N_3N_2N_1N_0$, LDAA N : load accumulator with the contents of memory location N.
- **0 1 0 0** $N_3N_2N_1N_0$, STAA N : store ACCA into memory location N.
- **0 1 0 1** $N_3N_2N_1N_0$, JMP N : jump to program address N.
- **0 1 1 0 X X X 0**, ADDA S : ACCA := ACCA + Sw + C.
- **0 1 1 0 X X X 1**, SUBA S : ACCA := ACCA - Sw - /C.
- **0 1 1 1** $N_3N_2N_1N_0$, ANDA N : AND the contents of N with ACCA and store in ACCA.
- **1 0 0 0 X X X 0**, CLC : clear carry bit (C = 0).
- **1 0 0 0 X X X 1**, SEC : set carry bit (C = 1).
- **1 0 0 1 X X X 0**, DECA : decrement ACCA.
- **1 0 0 1 X X X 1**, INCA : increment ACCA.
- **1 0 1 0 X X X 0**, RORA : rotate ACCA right (Q_3 := C and C := Q_0). (Note: In your circuit Q_3 is on the left whereas in the 74194 specs, Q_3 is considered to be the rightmost bit).
- **1 0 1 0 X X X 1**, ROLA : rotate ACCA left (Q_0 := C and C := Q_3).
- **1 0 1 1** $N_3N_2N_1N_0$, STSW N : (N) := Sw.
- **1 1 0 0** $N_3N_2N_1N_0$, JCS N : jump to program address N if carry set.
- **1 1 0 1** $N_3N_2N_1N_0$, JEQ N: jump to program address N if A = B.
  Note: ALU must be in subtract mode and CALU clear (borrow = 1) to make F = 1111 (AEB HIGH) when A = B. For these instructions, A = ACCA and B = switches (input).
- **1 1 1 0** $N_3N_2N_1N_0$, JMI N : jump to program address N if ACCA -ve ($Q_3 = 1$).
- **1 1 1 1 X X X 0**, CLRA : ACCA := 0000.
- **1 1 1 1 X X X 1**, SETA : ACCA := 1111.

5. Using the following memory module:

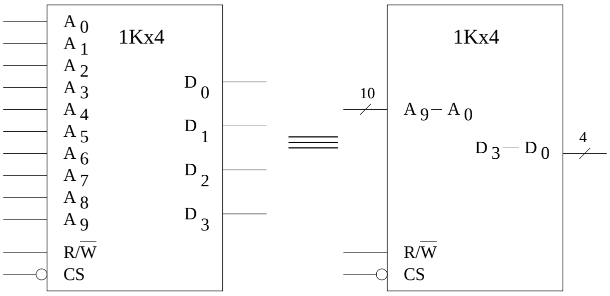


Figure 6: Memory module

(a) Design a memory circuit which will have 2 Kilo bytes of memory, (2K x 8). **(5 marks)**
Note: Standard TTL modules are available to be used in your design.

(b) Label the range of addresses for each module in the circuit using HEX values. **(2 marks)**

(c) The byte 4A HEX is written into the address 063A and read back as 48. Indicate which memory module is defective. **(2 marks)**

Question 5, Cont'd